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EXAMINER	
VIGUSHIN, JOHN B	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 02/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,659	MOSLEY, LARRY EUGENE	
	Examiner	Art Unit	
	John B. Vigushin	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-16 and 18-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-16 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of Referefices Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Rejections Based On Prior Art

1. The following references were relied upon for the rejections hereinbelow:

Ahn et al. (US 6,274,937 B1)	Tosaki et al. (US 6,272,020 B1)
Farooq et al. (US 6,228,682 B1)	Herrell et al. (US 6,191,479 B1)*
Giri et al. (US 6,037,044)	Naito et al. (US 6,034,864)*
Farooq et al. (US 6,023,407)*	Stone (US 5,530,288)

*References provided by Applicant in IDS filed as Paper No. 3 on February 13, 2002.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herrell et al.

As to Claims 13 and 14:

I. Herrell et al. discloses: a die 11 including an electronic system (col.4: 17-20); a capacitor 17 (consisting of conductive layers 13 and 14 separated by dielectric layer 18) coupled to die 11, the capacitor 17 is capable of decoupling a power supply connection at the die without additional capacitors located external to the die (col.2: 43-48; col.3:

28-30 and 36-39; col.5: 21-33); a dielectric layer 12 located between the capacitor 17 and die 11 (dielectric layer 12--shown in Fig. 1 but not addressed in the description of the Fig. 1 embodiment--is evidently the same type of dielectric layer as dielectric layer 15 in Fig. 1, described in col.4: 38-42, and is analogous to the dielectric layer 22 described in the Fig. 2 embodiment in col.8: 60-64).

II. Herrell et al. discloses a capacitor 17 with an "on-chip" thin-film structure formed on die 11 that enables an "extremely low inductance electrical pathway" between the capacitor 17 and die 11 (col.3: 36-39) but is silent as to the specific dimensions of the capacitor 17 and the dielectric layers 12 and 15 that contain the vias that establish the connections between the capacitor 17, and die 11 and bumps 16, respectively (col.4: 60-64; col.5: 3-7).

III. However, it would have been an obvious matter of engineering choice to one of ordinary skill in the art at the time the invention was made to set the thickness of dielectric layer 12 at less than about 0.1 mm from the die 11 (hence, the capacitor 17 would then be located less than about 0.1 mm from die 11), or, more specifically, between 0.05 mm and 0.1 mm, in order to ensure the shortest possible electrical pathway between the capacitor 17 and die 11, thus enabling an "extremely low inductance" in the resulting electrical connection therebetween, as explicitly taught by Herrell et al., and also because it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

4. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq et al. (US 6,023,407) in view of Stone and Ahn et al.

As to Claim 15:

I. Farooq et al. discloses a capacitor (i.e., an interposer capacitor shown in Fig. 10), employed between a first die and a circuit card (Abstract, lines 1-3; col.1: 54-59), and having a first (upper) surface having a controlled collapse chip connection (C4) 12 coupled to the first die and a second (lower) surface having a C4 12 coupled to the circuit card (col.7: 48-53).

II. Farooq et al. does not teach a second die to which the second (lower) surface of the (interposer) capacitor is coupled; rather, the second surface is coupled to the circuit card, as mentioned above.

IIIa. Stone discloses, in Fig. 2, a passive device interposer 100 which may be, *inter alia*, a capacitor interposer (col.6: 47-49 and 61-64) and further discloses that the capacitor interposer 100 is employed between any two devices 31 and 33 which may be, *inter alia*, circuit cards or chips or any combination of devices (col.8: 26-38).

IIIb. Ahn et al. discloses, in Fig. 1, an interposer 30 having built-in capacitors 110 (col.7: 14-45) and further discloses that interposer 30 is employed between a first die 20 and a second die 22.

IV. Since Farooq et al., Stone and Ahn et al. practice packaging electronic devices on capacitor interposers, wherein Stone teaches that the capacitor interposer may be employed between *any* two devices, including chips (e.g., IC dice), and Ahn et al. *specifically* teaches an embodiment wherein a capacitor interposer is employed

between a first die and a second die, then the use of the capacitor interposer between a first die and a second die would have been readily recognized in the pertinent art of Farooq et al. as a functional application of the capacitor interposer.

V. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the package of Farooq et al. by replacing the circuit card with a second die, as taught by Stone and Ahn et al. in order to meet the needs of a system that requires the benefit of noise decoupling or other filtering of signals to and from a first and a second die connected to opposite sides of the capacitor interposer, as taught by Stone and Ahn et al.

As to Claim 16:

I. Farooq et al., in view of Stone and Ahn et al., disclose all the limitations of base Claim 15, and modifying reference Ahn et al. further discloses that the first die 20 and second die 22 may be a microprocessor (col.6: 12-15) or may include a communication system (col.6: 17-19) but does not teach the special case wherein the first die 20 includes the processor and the second die 22 includes the communication system.

II. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify and enhance the functionality of Farooq et al., in view of Stone and Ahn et al., with an embodiment wherein the first die 20 (as shown in Ahn et al., Fig. 1) includes the disclosed microprocessor while the second die 22 (as shown in Ahn et al., Fig. 1) includes the disclosed communication system in

communication applications requiring signal processing and the execution of instructions for computing and communication functions.

5. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tosaki et al. in view of Naito et al. and Farooq et al. (US 6,228,682 B1).

I. Tosaki et al. discloses, in Fig. 3: a substrate 3 having a first surface and a second surface; a die 2 coupled to the first surface; a capacitor 4 is coupled to the second surface by solder bumps 8B (col.10: 3-10) and is electrically coupled to die 2 through substrate 3 (col.8: 60-62 and 65-67; col.9: 2-8).

II. Tosaki et al. does not teach that capacitor 4 has a plurality of vias coupled to a plurality of conductive layers in the capacitor, and does not teach that the capacitor solder bumps 8B are C4 (controlled collapse chip connection) solder balls.

IIIa. Naito et al. discloses, in Figs. 1, 2 and 2A, a multilayer capacitor 36 (col.4: 65-col.6: 5) having a plurality of vias 40, 41 coupled to conductive layers in the capacitor and to bumps 38, 39 on the outer surface 37 of capacitor 36 for connecting the capacitor 36 to a circuit substrate ensuring counter current flow in vias 40, 41, thereby reducing parasitic equivalent series inductance (ESL) (col.5: 12-18; col.9: 38-47).

IIIb. Farooq et al. discloses, in Fig. 1, a capacitor 10 electrically coupled to substrate 50 by C4 bumps 40 (col.1: 25-28; col.4: 13-21).

IVa. Since Tosaki et al. and Naito et al. both teach capacitors coupled to the second surface of the substrate by bump connections, then the plurality of vias coupled to the conductive layers in the capacitor and coupled to the bumps on the outer surface of the capacitor to reduce parasitic ESL in the capacitor circuit by ensuring counter

current flow in the vias, as taught by Naito et al., would have been readily recognized in the pertinent art of Tosaki et al.

IVb. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the capacitor of Tosaki et al. by including a plurality of vias coupled to a plurality of layers in the capacitor and to the bumps on the external surface of the capacitor (that electrically couple the capacitor to the substrate) in order to reduce the parasitic ESL contribution of the capacitor to the system circuit, as taught by Naito et al.

Va. Since Tosaki et al. and Farooq et al. both teach solder bump connections on the capacitor for coupling the capacitor to the substrate, then the use of C4 bumps, as taught by Farooq et al., for the purpose of obtaining a highly reliable coupling of capacitor to substrate, would have been readily recognized in the pertinent art of Tosaki et al.

Vb. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the capacitor solder bumps of Tosaki et al. with the C4 capacitor solder bumps of Farooq et al. that use the C4 technology to obtain a highly reliable coupling of the capacitor to the substrate, as taught in Farooq et al.

6. Claims 19 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tosaki in view of Naito et al. and Farooq et al. (US 6,228,682 B1), as applied to Claim 18 above, and further in view of Ahn et al.

As to Claim 19:

I. Modified Tosaki et al. teaches a CMOS-based die 2 mounted to interposer substrate 3 (col.1: 10-13; col.4: 60-61) but does not teach does not teach a specific type of die 2.

II. Ahn et al. discloses an interposer substrate 10 with CMOS based dice 20, 22 mounted thereon, wherein one of the die 20 and die 22 is a microprocessor (col.6: 12-15).

III. Since modified Tosaki et al. and Ahn et al. mount a die to an interposer, the use of a processor die, as taught by Ahn et al., would have been readily recognized as a useful and necessary component in certain electronic applications of modified Tosaki et al.

IV. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to further modify Tosaki et al. by having a processor die stand in as die 2 in Tosaki et al. in order to meet the needs of certain electronic applications that require computer functions, as taught by Ahn et al.

As to Claim 20:

I. Modified Tosaki et al. discloses, in Fig. 3, a capacitor 4 is electrically coupled to die 2 through the wiring of substrate 3, wherein capacitor 4 is mounted in a cavity 5 of substrate 3 in order that the wiring distance between the capacitor 4 and die 2 is as short as possible, thus reducing parasitic induction in the capacitor (col.7: 15-34).

II. Modified Tosaki et al. does not teach that the (bumped) surface of capacitor 4 is located less than about 0.1 mm from the (bumped) surface of die 2.

III. However, it would have been an obvious matter of engineering choice to one of ordinary skill in the art at the time the invention was made to design the chip mounting region of substrate 3 in modified Tosaki et al. such that the thickness of the die/capacitor mounting portion of substrate 3 allows the bumped surface of the capacitor 4 to be located less than about 0.1 mm from the bumped surface of die 2, since such a structure would ensure a short wiring distance in the substrate between the capacitor 4 and die 2, as taught by Tosaki et al., and since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

7. Claims 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Herrell et al. in view of Giri et al.

As to Claim 21:

I. Herrell et al. discloses a processor 11 (col.8: 24-29); and a single multilayered single package capacitor 17 coupled to the processor 11 and capable of decoupling a power supply from the processor (col.1: 12-24; col.4: 31-37; col.8: 29-31).

II. Herrell et al. does not teach that the processor 11 requires at least 5 watts of power to be operable but suggests that processor 11 is a high power processor because it operates at high peak currents of 50-100 Amperes or more (col.4: 31-37).

III. Giri et al. discloses a high power processor (chip) mounted on substrate 100, the high power processor operating at 50-100 watts (col.5: 22-26).

IV. Since Herrell et al. and Giri et al. package high performance processors and Herrell et al. operate at 50-100 Amperes or more, then it would have been an obvious matter of engineering choice to one of ordinary skill in the art at the time the invention was made to use a processor 11 in Herrell et al. that requires at least 5 watts of power to be operable, as taught by Giri et al., in order to enable the processor 11 of Herrell et al. to operate at peak currents of 50-100 Amperes or more as disclosed by Herrell et al., and furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a processor 11 in Herrell et al. that requires at least 5 watts of power to be operable, as taught by Giri et al., since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

As to Claim 22, modified Herrell et al. further discloses that the single multilayered single package capacitor 17 is capable of being mounted on a substrate by a plurality of solder bumps 16 (Fig. 1; col.4: 38-42).

As to Claim 23, modified Herrell et al. further discloses that the single multilayered single package capacitor 17 is capable of being mounted on a substrate using a controlled collapse chip connection (C4) (col.6: 14-25).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 703-308-1205. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David L. Talbott can be reached on 703-305-9883. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7382 for regular communications and 703-308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

John B. Vigushin
Examiner
Art Unit 2827

jbv
February 19, 2003